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## 1 The charge-share modified (CSM) precharge-level architecture for high speed and low-power ferroelectric memory

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##### 6 Charge-transferred presensing and efficiently precharged negative word-line schemes for low-voltage DRAMs

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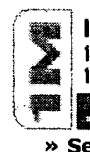


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*Hansoo Kim; In-Cheol Park;*  
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*Wicht, B.; Larguier, J.-Y.; Schmitt-Landsiedel, D.;*  
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40 **A 300 MHz multi-banked eDRAM macro featuring GND sense, bit-line twisting and direct reference cell write**

*Barth, J.; Anand, D.; Dreibelbis, J.; Nelson, E.;*  
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